`Faculty:	**FACULTY OF ELECTRICAL ENGINEERING**		
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FAKULTI KEJURUTERAAN ELEKTRIK
UNIVERSITI TEKNOLOGI MALAYSIA
KAMPUS SKUDAI
JOHOR

SKEL 3742
VLSI SYSTEM DESIGN LAB

Lab Project : VLSI Physical Design with OpenLane EDA

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VLSI Physical Design Lab (Labsheet)

Faculty of Electrical Engineering

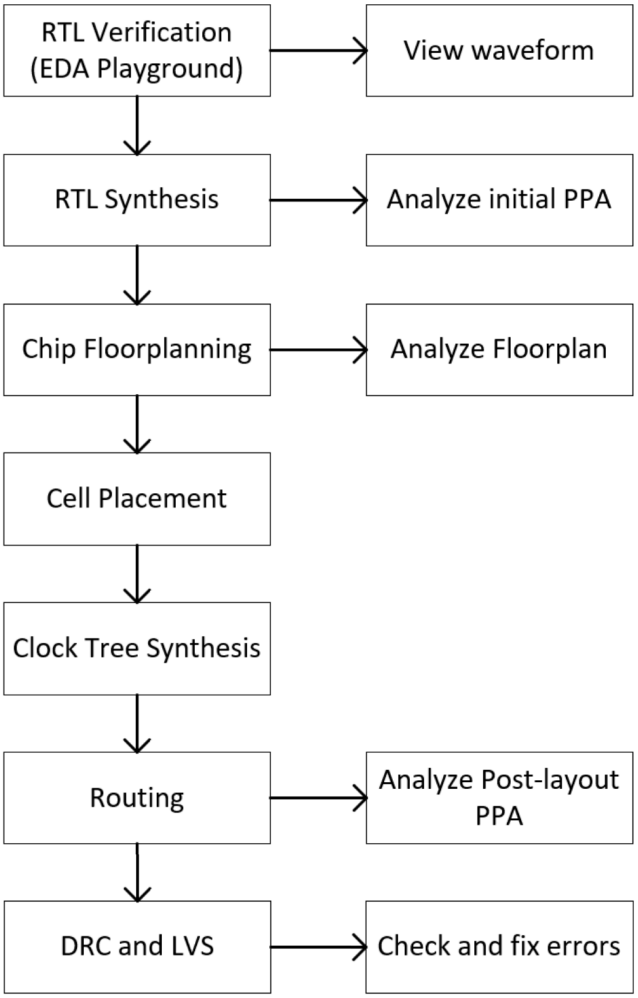
Universiti Teknologi Malaysia

Task

- Perform RTL design verification and implement a complete physical design of a baseline complex digital system, from RTL to GDS which includes synthesis, floorplanning, placement, routing, DRC, and LVS verifications.
- Modify the baseline design for different physical layout design parameters and/or constraints. Rerun physical implementation and compare PPA parameters between the baseline and your proposed modification. Some examples of modifications:
    - RTL design parameters
    - Synthesis constraint
    - Floorplan Aspect ratio
    - Floorplan utilization rate
    - Configurations of Power and Ground nets
    - Placement optimization options
    - Clock tree optimization options
    - Routing optimization options
- **IMPORTANT**: Make sure you achieved positive slacks in your timing analysis and that your designs are free from any DRC or LVS errors.
- Demo your chip design and show correct functionality and analysis for both the baseline and modified designs.
- Write a final report on your project.

Steps to complete the Project

1. The overall project flow is given below:



2. Obtain the RTL design specifications from your lab instructor.
3. Design a RTL testbench and verify the given RTL module using EDA Playground. Show the simulation results are correct using several feasible test patterns.
4. Perform RTL synthesis and analyze for initial PPA.
    - WNS (Setup)
    - WNS (Hold)
    - Dynamic Power
    - Leakage Power
    - Total Power
    - Number of combinational cells
    - Number of sequential cells

- Total number of cells

5. Perform chip floorplanning and determine the parameters.
    a. Chip width
    b. Chip height
    c. Chip area
    d. Chip aspect ratio
6. Perform cell placement, clock tree synthesis, and routing. Analyze for final PPA.
    a. WNS (Setup)
    b. WNS (Hold)
    c. Dynamic Power
    d. Leakage Power
    e. Total Power
    f. Number of combinational cells
    g. Number of sequential cells
    h. Total number of cells
7. Perform DRC and LVS verifications and report the results.
    a. Number of DRC errors
    b. DRC errors fixed
    c. Number of LVS errors
    d. LVS errors fixed
8. Perform modifications to your design (in any stage from steps 2 to 6) and compare the PPA and layout results with the baseline design.
9. In your demo and report, discuss the following:
    a. Is there any difference in PPA between post-synthesis and post-place and route designs? If so, why is this the case?
    b. What modifications have you made to the original baseline design? Are there any specific challenges faced in implementing the new design?
    c. Compare the PPA between baseline and new design. What have you improved in the new design compared to the baseline?