

Getting Started with Quartus

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Abstract

This article introduces the Quartus software, where to find it, install it and check out the installation with a simple design.

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1. What is Quartus

Quartus II is a software package for design and development of digital system based on Altera FPGA and CPLD devices. The main tasks simulation and verification activities. The designed model are simulated for functional and timing verification on Quartus II before integrated with the actual Altera devices for hardware verification. Quartus can also be used even without access to the actual Altera devices, if we only want to go up to the simulation level.

In this tutorial, Quartus II 13.1 Web Edition will be used. This software supports both 32-bits and 64-bits operating system. Users may also use other version that meet their system requirement and the targeting Altera device.

Quartus is available in versions 13.0sp1 through 20.4 (up to March 2021). All previous version are discontinued. Up until version 16, the software was called Quartus II. After Intel took over Altera in 2016, three changes were made:

- Intel branding in the software
- The Altera Quartus II is now called Intel® Quartus® Prime and Quartus II Web Edition become Quartus Prime Lite Edition
- Introduction of the Pro edition which supports the partial reconfiguration capability of the new Arria 10 FPGA

Table 1 summarizes the differences between pro and non-pro versions. As the version numbers get bigger, the software becomes more complex and require more computer resources. Version 13.0sp1 is the only version to support the Cyclone II low-cost FPGA. If you are not using Cyclone II, go for version 13.1. Install higher versions only if you installation problems with these two versions. Table 1. Quartus Prime editions.

Edition	Device Support	Cost
Pro Edition	Focus on top-of-the-line devices	30 day trial
Standard Edition	Widest device support	30 day trial
Lite/Web Edition	Entry-level	Free

2. Getting Quartus

This section shows the steps to download version 13.1 of Quartus II Web Edition.

The first step to downloading is to point your browser to http://fpgasoftware.intel.com/13.1/?edition=web.

intel.	PRODUCTS	SUPPORT	SOLUTIONS	DEVELOPERS	PARTNERS	8	USA (ENGLISH)	Q Search Intel.com
Home >	Downloads > 0	Quartus II Web	Edition					
Dow	nload Cei	nter for l	FPGAs					
	Design Softwar Embedded Soft Archives Licensing Programming Sof Drivers Board System DJ Board Layout and Legacy Softwar	tware esign et al.	Quartu Release data Latest Relea Select releas Operating S devices in like to reco devices in devices in devices in devices in devices in devices in devices in devices in devices in devices in devices in devices in device	s II Web Edit November, 2013 ex v20.4 ex 13.1 v rstem @ @@/ Vi artus II Web Edition this release are avail wire customer notific chived version and the the latest version. It to make the interpret offware, follow the y be exposed to a y	tion ndows O 🔬 Linux Design Software, Verra ations by e-mail, plea not include the latest device technical recomment unrenability issue if you	tion 13.1 is subject on, or all devices as functional and se substribt to or functional and se family. See functional family. See functional family. The functional family family family. The functional family family family family. The functional family family family family family. The functional family family family family family family family family family family family	to removal from th upported by this very a subscribe to surce carity updates. For a carity updates. For a carity updates. Tor a cari	evels when support for all assessment of the support for all supported version of Quartus. Supported version of Quartus. Construct, vois relief left or por mpatibility. If you must use this tus Prime Quartus II Design RUS solviton for more details.
			The Quantum And MAX 1	artus II Design Soft / devices; select Arri	ware Version, 13.1 sup a II and Cyclone V dev	ports the followin ices. <u>More</u>	ng device families: all	Cyclone III, Cyclone IV, MAX II,

Figure 1. Choose a version.

You can download the full Quartus II Web Edition bundle which is 4.4GB. This will download gigabytes worth of device support which you will never use.

Download Only the Necessary Files

Since you are going to use only the CPLD chip, it is better to download only the necessary files.

1. Choose the Individual Files tab as shown in Figure 2.

ownload and i	nstall instructions	• <u>More</u>			
ead Intel FPGA	Software v13.1 Insta	allation FAQ			
uick Start Guid	<u>e</u>			0	
					lates Available
Quartus II We	b Edition (Free)				
Quartus II	Software (include:	s Nios II EDS)			`
Size: 1.5 G	B MD5: 49E9F37AI	D4B99EE258F	11353F11A0A1D		0
ModelSim	-Altera Edition (ind	cludes Starter	Edition)		0
Size: 822.8	3 MB MD5: B97739	CAD5FA9BE4	156DFFC614AC9F26		•
Devices You must inst Arria II de Size: 466.	all device support f vice support 5 MB MD5: 35E5AC	or at least one	e device family to use the 2821C9E0C74E3A5B	e Quartus II softwar	re.
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Figure 2. Download the marked files.

- 2. Download Quartus II Software
- 3. ModelSim-Altera Edition
- 4. Download MAX II device support for using EPM240. Do not download any other files.
- 4. You will be asked to enter your password if you have not logged in. And you may have to create an account if you have not done so. If everything is fine, you will download less than 2.6 GB instead of 4.4 GB for the full package. You should have:

File	Size
QuartusSetupWeb-13.1.0.162.exe	1.58 GB
ModelSimSetup-13.1.0.162.exe	864 MB
max_web-13.1.0.162.qdz	6.4 MB

Installing Quartus

For installation, double-click on the *QuartusLiteSetup* executable file and choose the default values.

Start Designing Designing with Quarkus II software requires a project Create a New Project (read) Open Existing Project Open Recent Project:	Start Designing Designing with Quartus II software requires a project Create a New Project (New Project Wizard) Open Existing Project Open Recent Project	Getting Started With Q	uartus® II Software
Designing with Quartus II software requires a project Create a New Project (New Project Wizera) Open Existing Project Open Existing Project	Designing with Quartus II software requires a project Create a New Project (New Project Wizard) Open Existing Project Open Recent Project:	Start Designing	Start Learning
Open Existing Project Open Existing Project Open Recent Project:	Open Existing Project Open Recent Project: Open Recent Project:	Designing with Quartus II software requires a project	The audio/video interactive tutorial teaches you the basic features of Quartus II software
Open Recent Project:	Open Recent Project:	(New Project Wizard) Open Existing Project	Open Interactive Tutorial
		Open Recent Project:	
Web vs. Subscription Buy Subscription Literature Training Online Demos Sup		Don't show this screen again	

Figure 3. Quartus II Web Edition splash screen.

3. Designing with Quartus

Before you can start experimenting, you should understand how Quartus does its work. Figure 4 gives a overview. Note that Quartus software can do much more than what is shown here.



Figure 4. Design flow using Quartus.

The square boxes are Quartus editor or dialog boxes which you can use to enter designs or settings. They are:

- **Block diagram editor** for design entry using gates and logic blocks
- **Text editor** for design entry using hardware design language, usually Verilog
- State machine editor for entering a state machine
- **Waveform editor** for preparing an input waveform before simulation
- **Device assignment** is a simple dialog box to specify the target device
- **Pin assignment** is a dialog box for setting the input/output pins on the target device

The ovals are internal Quartus operations that execute commands:

- Compiler converts a design into a *netlist*
- Fitter configures the internal wiring on a target device to the netlist to obtain a *bitstream*
- Functional simulator performs *device-independent* simulation based on logic function only without considering the physical device aspects
- **Timing simulator** performs *device-specific* simulation which includes delay estimation. This simulation is slower than functional so it is usually done after a circuit has passed functional simulation.
- **Programmer** download the bitstream into the target device

For simple experiments with digital logic, only two boxes are used: the Block Diagram Editor and the Waveform Editor.

4. Example Design

This tutorial uses a simple circuit to check out the Quartus installation.

A combinational logic circuit shows the results for three people who vote. The three people are labeled as *A*, *B*, and *C*. If at least two of them vote yes, then the output *V* becomes HIGH. Else if only one or none of them vote yes, the output becomes LOW.

The truth table of the problem is given in Table 2.

	Table	2.	Voter	truth	table
--	-------	----	-------	-------	-------

	Inpu	Output	
Α	B	С	V
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

There are several possible Boolean equations that can be derived. After simplifying the equation for *V*, we get

$$V = AB + BC + AC$$

We will now enter this circuit in Quartus and simulate its function.

5. Specifying Project Settings

1. Launch Quartus by double-clicking on the icon.



Figure 5. Quartus II Web Edition welcome screen.

 From the top menu, choose File → New Project Wizard. This will bring us to the introduction page.

	New Project Wizard	×
Introduction		
The New Project Wiz	ard helps you create a new project and preliminary project settings, including the following:	
 Proju Nam Proju Targ EDA 	et name and directory e of the top-level degreentty et files and libraries et device family and device to device family and device	
You can change the the various pages of	settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can us the Settings dialog box to add functionality to the project.	e
Don't show me th	is introduction again	
	< Back Next > Finish Cancel Help	
	\sim	

Figure 6. New project Introduction page.

3. Click Next > . This brings us to page 1.

athank to also consultants alter alter alter alter alter a		N			
vnat is the working directory for this project	2	63			
C:/quartusprojects/voting					
vnat is the name of this project?					
voting					
Vhat is the name of the top-level design enti ame in the design file.	ity for this project?	This name is case	sensitive and must e	exactly match the	entity
voting					

Figure 7. Quartus II Web Edition welcome screen.

- Working directory is the location of your project files. We strongly suggest to change the directory settings to avoid problems if you have to reinstall Quartus and to make it easy for backing up your data. You can create a working directory at the root level of your hard disk (e.g. C:\quartusprojects) or inside your documents folder. Once you have decided on the working directory for all your Quartus projects, create a subdirectory for your current design (e.g. Voting).
- **Name** is the name of your project. Simply use the same name at the design directory.
- **Top level entity** specifies the master file in your design. Unless you have a specific reason, just use the project name.
- 4. Click Finish. Notice the voting entity as shown in Figure 8.

The Quartus program has 4 windows:

- **Project navigator**: displays the design files in your working directory and their relationships
- Tasks: shows the progress of design tasks
- Workspace: is the area where you enter the design
- Messages: displays messages from the tasks e.g. compiler, fitter, simulator



Figure 8. Quartus layout.

2

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Symbol Tool

6. Schematic Entry

In the design entry step you create a schematic or Block Design File (.bdf) that is the top-level design.

 From the top menu, choose File ⇒ New ⇒ Block Diagram/Schematic File to create a new file (see Figure 9) then click OK.



Figure 9. New BDF.

Figure 10. Quartus schematic editor.3. Click Symbol Tool. A pop-up dialog box will appear as shown in Figure 11.

Block 1.bdf

ירר

×

Orthogonal Node Tool

9 ° 2 6 8 6 8 6 9 7 °

braries:		
⊕ and3 ⊕ and4 ∨ ↓ and4 ∨ ↓ and4 → and4	Had Had	
and2		
Repeat-insert mode		
Launch MegaWizard Plug-In		

Figure 11. Add new symbol.

- 4. Expand c:/altera/13.0/quartus/libraries, expand primitives followed logic.
- 2. The schematic entry window will appear on the working space as shown.

- 5. Select and2 and then check Repeat-insert mode and then click OK.
- 6. Place the three (3) and2 gates as shown in Figure 12 by clicking on the desired placing area and then press the $\boxed{\text{ESC}}$ keyboard key to return back to the default arrow cursor.



Figure 12. Add 3 and 2 gates.

7. Another way to add symbols is by clicking anywhere on the schematic editor working space. The Symbol dialog box similar to Figure 11 will appear. At this time, insert an or3 gate as shown in Figure 13.





8. Next we will add the input/output pins. In the Symbol dialog box, expand

c:/altera/13.0/quartus/libraries, expand
primitives followed by pin.

9. Select input then $\operatorname{click}(\operatorname{OK})$.

Ubraries:	nbol	
Name:	tes: Cri/letra/13.0/quartus/foraties/ ∧ Compasfunctions Conters Conters Conters Conters Conter	SI A
insuit a		
Repeat-insert mode Insert symbol as block	epeat-insert mode	
Launch MegaWizard Plug-In MegaWizard Plug-In Manager	aunch MegaWizard Plug-In MegaWizard Plug-In Manager	

Figure 14. Adding an input pin.

- 10. Place the three (3) unit **input** pins.
- 11. Repeat step 9 and 10 for an **output** pin. By now we should have our design entry such shown in Figure 15.

pin name	AND2	
pin name	AND2	OUTPUI pin name
pin name	AND2	

Figure 15. All gates entered.

12. Right-click on the top most input pin and click on Properties. We should see a Pin Properties pop-up dialog box (Figure 16).

-					
To create multip (For example: "i	ie pins, enter a nam name[30]"), or ent	ter a comma-seper	tation rated list of nar	mes.	
Pin name(s):	A]		
Default value:	VCC				•

Figure 16. Pin Properties dialog box.

- 13. Rename the pin name as *A*. By default, the default value will set to VCC if not, select VCC as shown in Figure 16. Click OK.
- 14. Repeat the Step 13 for pin *B* and *C* and output pin *V*
- 15. Using the Orthogonal Node Tools on the schematic toolbars Make the circuit connection for the Boolean equation. We should see the schematics similar to Figure 17.



Figure 17. All pins renamed, and gates connected.

16. From the top menu, choose **File Save As...**

Save As				×
Save in:	voting	•	← 🗈 💣 📰▼	
Quick access Desktop Libraries This PC	Name	^	Date modified 30/1/2019 12:20 PM	Type File folder
	<			>
	File name: Save as type:	voting Block Diagram/Schematic Files (*.t. I Add file to current project	▼	Save Cancel

Figure 18. Save the file.

18. From the top menu, choose Processing → Start Compilation
We can also simply click on Start Compilation button on the toolbar. The compilation report is shown in Figure 19. For this tutorial, ignore all warnings. Click OK.

voti	ng.bdf		\times		Compilation
Flow Summary					
Flow Status	Successful - Fri Feb (01 21:44:57	2019		
Quartus II 64-Bit Version	13.0.0 Build 156 04/2	24/2013 SJ V	Neb Edition		
Revision Name	voting				
Top-level Entity Name	voting				
Family	MAX II	😂 Quart	us II		×
Device	EPM240T100C5				
Timing Models	Final		Full Compi	lation was succe	sstul (11 warnings)
Total logic elements	1 / 240 (< 1 %)				
Total pins	4 / 80 (5 %)				
Total virtual pins	0				ОК
UFM blocks	0/1(0%)				2

Figure 19. Compilation success.

7. Simulation

In order to simulate the design, we will enter the input simulation waveform.

1. Choose File \Rightarrow New \Rightarrow University Program VWF to create a new file (see Figure 20) then click OK.



Figure 20. Create new waveform file.

2. Simulation waveform editor window will appear such shown in Figure 21.

ile Eile	Simulation \ Edit <u>V</u> iew	Naveform E Simulation	ditor - (<u>H</u> elp	C:/quartusproj v	iects/voting/votin	g - voting - [Wa	weform.vwf]*	Search altera] ×
B	€, X	0 <u>1</u> <u>z</u>	(\underline{L})	$\underline{\mathbb{M}} \hspace{0.1 cm} \backslash \underline{\underline{c}} \hspace{0.1 cm} \backslash \underline{\mathbb{Q}}$	X2 XB 🗞 🗞	為 📷 號			
Mast	er Time Bar:	0 ps	•	Pointer	604.81 ns Inte	erval: 604.81 ns	Start: 0 ps	End:	0 ps
	Name	Value at 0 ps	0 ps 0 ps	160,0 ns	320.0 ns	480,0 ns	640,0 ns	800,0 ns	960.0 ns ^

Figure 21. Blank waveform.

3. Go to **View ➡ Fit in Window** to get the Vector Waveform at the workspace. We can also adjust the view at our convenience through Zoom In and Zoom Out tool. Go to Edit → insert and click insert node or bus. A pop-up dialog box will appear as shown in Figure 22.

🅞 Insert N	Node or Bus	×
Name:		ОК
Type:	INPUT -	Cancel
Value type	9-Level 🔻	
Radix:	Binary -	Node Finder
Bus width:	1	- •
Start inde>	0	
Display	gray code count as binar	y count

Figure 22. Insert node dialog.

🎕 Node Finde	r					×
Named: *		Filter	: Pins: all		•	ОК
Look in: *					List	Cancel
Nodes Found:			Selecte	d Nodes:		
Name in_ A in_ B in_ C out V	T Input Input Input Output	Гуре	N N A N B C Copy all C	ame	T Input Input Input ed Nodes list	уре

Figure 23. Node finder dialog.

- 6. Follow these steps:
 - (a) Set the Filter to Pins:all
 - (b) Click List
 - (c) Click the >> button
 - (d) Click OK on the Node Finder window

🅞 Insert N	Node or Bus	×
Name:	**Multiple Items**	ок
Туре:	**Multiple Items** •	Cancel
Value type	9-Level 🔻	
Radix:	Binary -	Node Finder
Bus width:	1	
Start inde>	0	
Display	gray code count as bina	ry count

Figure 24. Adding multiple nodes.

7. We will be brought back at the Insert Node or Bus box as shown in Figure 24, click OK. By stage we will see voting inputs *A*, *B* and *C* all goes LOW at time 0ns to 100ns while voting output "V" is the output to be determined as shown in Figure 25.

	Name	Value at 0 ps	0	ps ps			1	160	0,0	n	s				32(0 <mark>,</mark> 0	ns	5			48	80,	0 r	ıs			(54(0 <mark>,</mark> 0	ns	5			80	00,	0 r	IS			90	<u>50</u> .	0 n	IS
in_	A	во			I				1		1					I				I				1				1	I			1					T				T		
<u>is</u> _	в	B 0			i					l						i				l									i			1									-		
<u>in</u>	С	B 0			1						L					1				ł									1									L					
out 	v	вх	×	×	×	~	ò	~	8	8	8	8	8	X	×	×	\times	×	×	Ş	ò	\gtrsim	*	×	*	Ņ	Ş	×	×	×	×	ò	Š	~	×	X	×	ò	\diamond	*	×	\gtrsim	Š

Figure 25. Waveform after inserting nodes.

8. Highlight *A* by clicking on the input port symbol of the port name (Figure 26.

	Name	Value at	0 ps	160,0 ns	320.0 ns	480,0 ns	640.0 ns	800,0 ns	960.0 ns ^
	Hame	0 ps	0 ps						
in_	A N	B 0							
in_	B	B 0							
<u>in</u>	с	B 0							
out	v	вх	\times	********	******	******	*******	*******	~~~~~

Figure 26. Waveform after selecting input A.

9. Click the Overwrite Clock icon on the toolbar and set the period of signal *A* to 1000 ns.

V2 V2 V2 v2 v2 ↓ Overwrite Clock	
Clock	×
Base waveform on time	period
Period: 1000	ns 🔻
Offset: 0.0	ns 💌
Duty cycle (%) 50	\$
ок	Cancel

Figure 27. Set period of B to 1000 ns.

10. Click input port symbol of input *B* to highlight the whole frame of input *B* as shown in Figure 28.

		Value at	0 ps	160,0 ns	320.0 ns	480,0 ns	640.0 ns	800,0 ns	960.0 ns
	Name	0 ps	0 ps						
₿-	A	в о							
3-	в	во							
3-	c	B 0							
ut 🗎	v	вх	××××	~~~~~~~~	******		*******	~~~~~~~	~~~~~

Figure 28. Waveform after selecting input B.

10. Next, click overwrite clock icon on the toolbar. popup window will appear as shown in Figure 29 fill in period 500ns then click OK.

Clock	×
Base waveform on time	period
Period: 500	ns 🔻
Offset: 0.0	us 🔻
Duty cycle (%) 50	
ок	Cancel

Figure 29. Set period of B to 500 ns.

11. Click port symbol of input *C* to highlight the whole frame of the input *C* as shown in Figure 30.

	Name	Value at 0 ps	0 ps 0 ps	160,0 ns	320,0 ns	480,0 ns	640.0 ns	800,0 ns	960.0 ns ^
in_	A	в 0							
in_	В	B 0							
in_	c 📐	B 0							
out 	V	вх	\times	*******	~~~~~	******	******	******	~~~~~

Figure 30. Waveform after selecting input C.

Next, click a pop-up box will appear as shown in Figure 31. Fill -up transition occurrence to count every 125ns, click OK.

🚭 Clock	×
Base waveform on time	period
Period: 250	ns 🔻
Offset: 0.0	ns 🔻
Duty cycle (%) 50	-
ок 🔓	Cancel

Figure 31. Set count to 125 ns.

13. Go to File click Save as. A pop-up box will appear as shown in Figure 32, click Save

Save Vector Wave	form File			×
Save in:	l voting		• • • • •	
Quick access Desktop Libraries This PC	Name db incremental_u output_files simulation	db	Date modified 29/1/2019 4:40 PM 29/1/2019 4:39 PM 29/1/2019 4:40 PM 29/1/2019 4:39 PM	Type File folder File folder File folder File folder
	<			>
	File name: Save as type:	Voting University Program VWF (*.vwf)	•	Save Cancel

Figure 32. Save the vector waveform.

- 14. Click run functional simulation icon on the toolbar. If the simulation is successful, a new window will appear showing the result of simulated waveforms.
- 15. With corresponding input *A*, *B* and *C*, notice that *V* is responding in accordance to our Boolean equation. Therefore, out design is now functional verified.

	Name	Value at 0 ps	0 ps 0 ps	160.0 ns	320 _, 0 ns	480,0 ns	640,0 ns	800 _, 0 ns	960.0 ns ^
in_	A	во							
in_	В	B 0							
<u>is</u> _	с	B 0							
out	v	B 0							

Figure 33. Functional simulation output.

16. Next, click run timing simulation icon on the toolbar the result as indicated in Figure 34. For simple simulations such as this circuit, timing requirements is not important. However, timing requirements are critical in more complex designs.

	Name	Value at 0 ps	0 ps 0 ps	160.0 ns	320,0 ns	480,0 ns	640.0 ns	800,0 ns	960.0 ns ^
in_	A	B 0							
<u>in</u>	В	B 0							
₿-	С	B 0						٦۲	
<u>99</u>	v	вх	<u> </u>						

Figure 34. Timing simulation output.

If we look closely or if we zoom in, we can see the difference at the V output. In the functional simulation output, V changes immediately after receiving input changes. In the timing simulation, there is some delay.

Acknowledgments

Thanks to Siti Nursyuhada binti Mahsahirun and Zulkifli Md. Yusof, both of Faculty of Manufacturing, Universiti Malaysia Pahang.

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