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SEEL3742

# FAKULTI KEJURUTERAAN ELEKTRIK UNIVERSITI TEKNOLOGI MALAYSIA KAMPUS SKUDAI JOHOR

## MICROELECTRONICS LABORATORY STUDENT PACK

## **Device Simulation and Characterization of an n-channel MOSFET**

Prepared by :

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: 14 March 2024

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### Project Introduction

Moore's law states that improving transistor performance, such as faster speed, smaller chip size, and lower power usage, is closely linked to scaling. Nevertheless, when the complementary metal oxide semiconductor (CMOS) transistor's channel length is reduced to sub-100 nm, it causes short channel effects (SCEs), which include the threshold voltage roll-off and the drain-induced barrier lowering (DIBL). To address these limitations, various advanced process techniques are introduced, including lightly doped drain (LDD), halo implantation, and retrograde well doping in the transistor's channel.

One issue that arises when scaling MOSFET devices is channel doping. If the channel is doped too lightly to achieve a low threshold voltage, punch-through can occur. As a result, channel doping needs to be increased, and oxide thickness must be reduced to address this issue while still maintaining sufficient inversion charge in the channel. However, reducing channel length and increasing substrate doping lead to another short channel effect known as impact ionization, where the drain/channel junction is reverse biased, and higher doping leads to a greater critical electric field in the device's channel region.

#### 1. Objectives

This laboratory is focused on the device characterization of an n-channel metaloxide semiconductor field-effect transistor (n-MOSFET). NanoHUB software is used as the primary tool for the simulation work. NanoHUB will simulate the n-MOSFET device structure and device characteristic (I-V curve).

The objectives of this project are:

- 1. To simulate a device structure of an n-MOSFET using 90 nm technology and obtain its current-voltage curve (I<sub>D</sub>-V<sub>D</sub> and I<sub>D</sub>-V<sub>G</sub>).
- 2. To study the effect of channel length reduction on the device performance.
- 3. To characterize the electrical parameter of the n-MOSFET.
- 4. To optimize the device performance by changing the physical dimension/structure to reduce the short channel effects (SCEs).

### 2. Project Task

Suppose you are working in a semiconductor company that produces integrated circuit (IC) chips. As an engineer in the research and development (R&D) unit, you are assigned a specific task to investigate the performance of 90 nm CMOS as the next potential nanoscale device before being implemented into actual fabrication and mass production process. Many design aspects must be considered when the MOSFET device is scaled down into nanoscale regime. As channel length is scaled to smaller dimensions, gate oxide must be reduced in thickness. Due to these, the short channel effect and leakage problem become more significant and thus introduce a big challenge to increase the transistor's electrical performance.

You have decided to start with the simulation of an n-type MOSFET.

### 3. Instruction:

- 1. Simulate a MOSFET device structure by using MOSFET simulator on nanoHUB.org (<u>http://nanohub.org/resources/mosfet</u>). Before you can use the simulator, please sign up for the NanoHUB.
- 2. Follow the lab sheet on how to get started with NanoHUB (see **Appendix 1**).
- 3. Simulate the n-channel MOSFET device structure and fill up the device parameters according to the lab task given (see **Appendix 2**).
- 4. Take the reading of I-V curves (for both  $I_D$ -V<sub>D</sub> and  $I_D$ -V<sub>G</sub>) which you can download the .csv data.
- 5. Compile the schematic of the n-MOSFET device structure, the related I-V curves plots (for both I<sub>D</sub>-V<sub>D</sub> and I<sub>D</sub>-V<sub>G</sub>), the electrical properties (V<sub>th</sub>, SS, I<sub>on</sub> and I<sub>off</sub>) for the n-channel MOSFET by using Origin or Matlab or any suitable software into word document together with all your results.
- 6. The electrical parameter for threshold voltage (V<sub>TH</sub>), subthreshold slope (SS), drain-induced barrier lowering (DIBL), and on-current (I<sub>ON</sub>) and off-current (I<sub>OFF</sub>) are as follows:

From the Log I<sub>D</sub>-V<sub>G</sub> plot, (V<sub>D1</sub> = 0.05V for linear region and V<sub>D2</sub> = 1.0V for saturation region).

- > Threshold voltage,  $V_{th} = V_G @ I_D = 10^{-6} A$  for  $V_{D2} = 1.0 V$ .
- Subthreshold slope, SS =  $\Delta V_G @$  the steepest 1 decade.
- > Leakage current,  $I_{off} = I_D @ V_G = 0V$  for  $V_{D2} = 1.0V$ .
- > On saturation current,  $I_{on} = I_D @ V_G = V_{max} = 1V$  for  $V_{D2} = 1.0V$ .
- > Drain-induced barrier lowering, DIBL = (V<sub>th</sub> @ V<sub>D1</sub> =  $0.05V V_{th}$  @ V<sub>D2</sub> = 1.0V) / ( $\Delta V_D$ ).
- 7. Please follow the timeline given in **Appendix 3** to complete your 3 weeks of the laboratory.

#### Appendix 1 (Lab sheet)

- 1. Sign up to NanoHub: <u>http://nanohub.org/resources/mosfet</u>
- 2. The GUI looks like this for the first tab menu: Structure Properties.
- 3. The red boxes are the device parameters that you should be focused on for your Lab Task. (Note: Other parameters which are not in the red boxes, keep it the same as the default value)
- 4. For this exercise, just leave it all as by Default value.

MOSFet (11:25 pm)	🗙 Terminate 🗼 Keep for later
Structural Properties   Model   Voltage Sweep	Simulate new input parameters
Device Type: MOSFET n-type	MOSFET tool (v. 1.0padre)
Doping Profile: Uniform Doping Density	Learn about Metal Oxide Semiconductor Field Effect Transistors (MOSFET) as you explore the devices in this simulator.
Source/Drain Nodes: 15 + - Channel Length: 100nm	input values for the various parameters on the left and click "Simulate" at the top to run the simulation. (Note: After the simulation has finished, 3D plots may still take some more time to load.)
Channel Nodes: 22 + -	Parameters
Oxide Thickness: 2nm Oxide Nodes: 5 + -	<ul> <li>Structural Properties General properties of the materials used, such as physical dimensions and doping.</li> </ul>
Junction Depth: 20nm	- Model
Junction Nodes: 30 + - Substrate Thickness: 50nm	loggle simulation parameters to take certain physical phenomena into account, such as impact ionization, at the sacrifice of computation speed. Also define the effects the surroundings have on the
Device Width: 1000nm	device, including temperature. - Voltage Sweep Define the effects the surroundings have on the device.
$ -L_{SD} -  -L_G -  -L_{SD} -  $	including applied voltage.
	MOSFET model notes:
Substrate	<ul> <li>V_substrate, the voltage applied to the substrate is tied to the source and is always grounded. The user can vary the gate and drain voltage, with respect to ground, in this simulation model.</li> <li>The entire device, except the oxide layer, is simulated as silicon</li> </ul>
Storage (manage)	🖌 🔀 🍢 782 x 602
← L <sub>SD</sub> → ← L <sub>G</sub> - Gate ↓ 7 <sub>0×</sub> Source Channe	$ \begin{array}{c} \bullet \bullet \bullet & \bullet \\ \bullet & \bullet \\ \bullet & \bullet \\ \bullet & \bullet \\ \hline \\$
Substra	ite
Source Doping Concentration	n: 2e+20/cm3
Drain Doping Concentration	n: <b>2e+20/cm3</b>
Channel Doping Concentration	n: 1e+18/cm3

Substrate Doping Concentration: 5e+16/cm3

- 5. Click on the second tab menu. The GUI looks like this for the second tab menu: Model.
- 6. The red boxes are the device parameters that you should be focused on for your Lab Task. (Note: Other parameters which are not in the red boxes, keep it the same as the default value)
- 7. For this exercise, just leave it all as by Default value.

MOSFet (11:25 pm)	🗙 Terminate 🖙 Keep for later
Structural Properties Model Voltage Sweep	Simulate new input parameters
Ambient Temperature: 🛑 300K 👻	
Gate Electrode: n+ poly silicon	MOSFET tool (v. 1.0padre)
Gate Electrode Workfunction: 0eV	Learn about Metal Oxide Semiconductor Field Effect Transistors (MOSFET) as you
Silicon parameters	explore the devices in this simulator.
Silicon Bandgap at 300K: 1.12eV	the left and click "Simulate" at the top to run
Silicon Dielectric Constant: 11.8	the simulation. (Note: After the simulation has finished, 3D
Electron Saturation Velocity: 1.03e+07cm/s	Poromotoro
Beta: 2	Structural Properties
Electron Mobility: 1400cm2/Vs	General properties of the materials used,
Oxide Parameters	- Model
Oxide Barrier Height at 300K: 3.4eV	Toggle simulation parameters to take certain physical phenomena into account such as
Oxide Dielectric Constant: 3.9	impact ionization, at the sacrifice of computation speed
Oxide Fixed Charge Density (/cm3): 0	Also define the effects the surroundings have on the device, including temperature.
Concentration dependent ionized impurity scattering: 💿 📄 yes	- Voltage Sweep
Vertical field dependent mobility model: 💿 📑 yes	Define the effects the surroundings have on the device, including applied voltage.
Parallel electric field dependence: 🥃 📑 yes	MOSFET model notes:
Impact ionization : 💿 페 🛄 no	- V_substrate, the voltage applied to the
Solve bipolar carriers: 💿 📰 🛄 no	grounded. The user can vary the gate and
Choose the transport model: Drift_Diffusion 💌 🔽	oran vollade with respect in dround in this
Storage (manage) 22% of 10GB	<ul> <li>✓ C 5 782 x 602</li> </ul>

- 8. Click on the third tab menu. The GUI looks like this for the third tab menu: Voltage Sweep.
- 9. The red boxes are the device parameters that you should be focused on for your Lab Task.
- 10. For this, please tick "yes" for Plot I-Vd Characteristic. Other value, just leave it all as by Default value.

MOSFet (11:25 pm)	🗙 Terminate 🕩 Keep for later
Structural Properties Model Voltage Sweep	Simulate new input parameters
I-Vg Plot         Plot Transfer Characteristic:         Vg Minimum:         Image: Sweep         Vg Minimum:         Image: Sweep         Vg Minimum:         Image: Sweep         Vg Maximum:         Image: Sweep         Vg Minimum:         Image: Sweep         Vg Maximum:         Image: Sweep         Vd Bias Minimum:         Image: Sweep         Vb Bias Point:         Image: Sweep         Vd Bias Maximum:         Image: Sweep         Vg Bias Minimum:         Image: Sweep         Vg Bias Maximum:         Image: Sweep         Vb Bias Point:         Image: Sweep         Image: S	MOSFET tool (v. 1.0padre) Learn about Metal Oxide Semiconductor Field Effect Transistors (MOSFET) as you explore the devices in this simulator. Input values for the various parameters on the left and click "Simulate" at the top to run the simulation. (Note: Affer the simulation has finished, 3D plots may still take some more time to load.) Parameters: - Structural Properties General properties of the materials used, such as physical dimensions and doping Model Toggle simulation parameters to take certain physical phenomena into account, such as impact ionization, at the sacrifice of computation speed. Also define the effects the surroundings have on the device, including temperature Voltage Sweep Define the effects the surroundings have on the device, including applied voltage. MOSFET model notes: - V_substrate, the voltage applied to the substrate is tied to the source and is always grounded. The user can vary the gate and drain voltage, with respect to ground, in this simulation model The entire device, except the oxide layer, is simulated as silicon
Storage (manage) 22% of 10GB	<ul> <li>✓ C <sup>™</sup> 782 x 602</li> </ul>

11. Go back to first tab menu: Structural Properties. Once all the parameter values have been set, to run the simulation, click "Simulate" button.

MOSFet (11:25 pm)	🗙 Terminate 🕩 Keep for later
Structural Properties Model Voltage Sweep	Simulate new input parameters
Device Type: MOSFET n-type Doping Profile: Uniform Doping Density Source/Drain Length: 50nm Source/Drain Nodes: 15 Channel Length: 100nm Channel Nodes: 22 Channel Nodes: 22 Oxide Thickness: 2nm Oxide Nodes: 5 Junction Depth: 20nm Junction Nodes: 30 Substrate Thickness: 50nm Substrate Nodes: 10 Device Width: 1000nm $\leftarrow L_{SD} \rightarrow \leftarrow L_{G} \rightarrow \leftarrow L_{SD} \rightarrow \leftarrow$ Gate Tox Source Channel Drain $D_{JUNC}$	<ul> <li>MOSFET tool (v. 1.0padre)</li> <li>Learn about Metal Oxide Semiconductor Field Effect Transistors (MOSFET) as you explore the devices in this simulator.</li> <li>Input values for the various parameters on the left and click "Simulate" at the top to run the simulation. (Note: After the simulation has finished, 3D plots may still take some more time to load.)</li> <li>Parameters:         <ul> <li>Structural Properties General properties of the materials used, such as physical dimensions and doping.</li> <li>Model</li> <li>Toggle simulation parameters to take certain physical phenomena into account, such as impact ionization, at the sacrifice of computation speed.</li> <li>Also define the effects the surroundings have on the device, including temperature.</li> <li>Voltage Sweep Define the effects the surroundings have on the device, including applied voltage.</li> </ul> </li> <li>MOSFET model notes:         <ul> <li>V_substrate, the voltage applied to the substrate is tied to the source and is always grounded. The user can vary the gate and drain voltage, with respect to ground, in this simulation model.</li> <li>The entire device, except the oxide layer, is simulated as silicon</li> </ul> </li> </ul>
Storage (manage)	✓ C 582 x 602

- 12. The results of the simulation will be appeared. 13. For  $I_D$ -V<sub>D</sub> curve, choose Id-Vd Characteristics.



14. For  $I_D$ -V<sub>G</sub> curve, scroll down menu and choose Id-Vg Characteristics. The graph is in Log scale  $I_D$ -V<sub>G</sub> curve.



15. Click on the green arrow to get the data in .csv file. Click Download. You can replot your graph.



- 16. Analyze the electrical parameters. From the Log  $I_D$ -V<sub>G</sub> plot, (V<sub>D1</sub> = 0.05V for linear region and V<sub>D2</sub> = 1.0V for saturation region).
  - > Threshold voltage,  $V_{th} = V_G @ I_D = 10^{-6} A$  for  $V_{D2} = 1.0 V$ .
  - > Subthreshold slope, SS =  $\Delta V_G @$  the steepest 1 decade.
  - > Leakage current,  $I_{off} = I_D @ V_G = 0V$  for  $V_{D2} = 1.0V$ .
  - > On saturation current,  $I_{on} = I_D @ V_G = V_{max} = 1V$  for  $V_{D2} = 1.0V$ .
  - > Drain-induced barrier lowering, DIBL = (V<sub>th</sub> @ V<sub>D1</sub> =  $0.05V V_{th}$  @ V<sub>D2</sub> = 1.0V) / ( $\Delta V_D$ ).

#### Appendix 2 (Lab Task)

1. In this lab task, you are required to simulate three generations (varying 3 channel lengths) of devices with parameters specified in Figure 1 and Table 1 without impact ionization included in the model, and set the voltage sweep as Default.



Figure 1: MOSFET Device structure.

Device	Channel Length (nm)	Oxide thickness (nm)	Source/Drain Doping (cm <sup>-3</sup> )	Channel Doping (cm <sup>-3</sup> )	Substrate Doping (cm <sup>-3</sup> )	Gate electrode	Vg V <sub>DD</sub> (V)		
1	100	3	2 x 10 <sup>20</sup>	10 <sup>18</sup>	10 <sup>17</sup>	N+ Polysilison	Default		
				10		N+	Default		
2	60	2	2 x 10 <sup>20</sup>	1018	6 x 10 <sup>17</sup>	Polysilicon	value		
3	45	2	2 x 10 <sup>20</sup>	10 <sup>18</sup>	1018	1018	6 x 10 <sup>17</sup>	N+	Default
			2 X 10		0 × 10	Polysilicon	value		

- 2. From the simulation results obtained, answer the following questions:
  - a. Find the electrical properties for all the devices such as V<sub>th</sub>, I<sub>on</sub>, I<sub>off</sub>, SS and DIBL for all the devices. Are all these devices well-designed, Yes or No? Please justify your answer with either Yes or No.
  - b. From your observations and results of Device 3, what causes the I-V characteristics to behave differently from Devices 1 and 2. Discuss this phenomenon and please suggest how to overcome the issues.

- For your next task, you need to do an optimization for Device 3, your 45 nm device should obtain the value of threshold voltage (V<sub>TH</sub>) approximately of V<sub>TH</sub> ≤ 0.3V and subthreshold slope, SS ≤ 85mV/dec. Not only that, but you also need to optimize other parameters such as DIBL and I<sub>ON</sub>/I<sub>OFF</sub> ratio.
  - a. There are several methods to optimize the device structure. Tips: you can try to alter this physical parameter of the device structure such as:
    - Oxide thickness
    - Substrate doping
    - Source/Drain Doping
    - Channel Doping
    - Gate Electrode
    - Or you can also use different Device types for example Double Gate MOSFET, SOI MOSFET, or any other device type that is available in the NanoHUB software.
  - b. Simulate the I-V characteristics (for both I<sub>D</sub>-V<sub>D</sub> and I<sub>D</sub>-V<sub>G</sub>) of the optimized Device 3 and analyze the electrical parameters. Comment on the results obtained and justify the method that you choose for the optimization.

## Appendix 3 (Timeline)

<u>Week</u>	<u>Task</u>	<u>Interview</u>	Submission Date
<u>1</u>	<ul> <li>i. Understand the Lab instruction.</li> <li>ii. Follow the Lab sheet (Appendix 1). Simulate the I-V curves. Do characterization of the electrical parameter. Find Vth, Ion, Ioff, SS, and DIBL.</li> <li>iii. Understand the Lab task (Appendix 2). Complete tasks No. 1 to 2.</li> <li>iv. Prepare Group proposal for task No. 3.</li> <li>v. Prepare Individual Short Report.</li> </ul>	Respective Member	For Group Proposal and Individual short Report: Week 2
<u>2</u>	<ul> <li>i. Submit Group Proposal and Individual Short Report.</li> <li>ii. Start to simulate task No. 3.</li> <li>iii. Simulate the I-V curves. Do optimization and characterization of the electrical parameter. Find V<sub>th</sub>, I<sub>on</sub>, I<sub>off</sub>, SS, and DIBL.</li> </ul>	Respective Member	-
<u>3</u>	<ul> <li>i. Continue simulation work.</li> <li>ii. Group Demo. Present your results for optimized Device 3. Make a comparison between before and after optimization for Device 3.</li> <li>iii. Finalize Long Report.</li> </ul>	Respective Member	For Long Report: A week after Week 3.

#### **Guideline for Long Report**

- ✓ Students must be able to present the report with all the required contents. Information is very organized, clear, and unambiguous with no mistakes. The report is orderly and visually appealing with no grammatical or spelling errors. All tasks were completed.
- ✓ The report follows the format (Outline: Abstract, Introduction/ Theory, Procedure, Data & Results, Discussion, Conclusion, and References).
  - 1. Abstract
    - Must include the background, the problem statement, the objective, the methodology, and the significant findings.
  - 2. Introduction/Theory
    - Background of problem/project.
    - > The approach taken in solving the problem/project.
    - Introduction to MOSFET and advanced MOSFET devices and short-channel effects.
    - Design criteria of the MOSFET and advanced MOSFET device structures (depending on your choice of the optimized device).
  - 3. Procedure
    - Emphasis on the lab procedure. Steps taken or methods used in conducting the simulation that can solve the problem/project.
    - > May also include NMOSFET structure, parameters, characteristics etc.
    - > Manual determination from graphs or equations
  - 4. Objective
    - > Objectives of the work (in the student's own words).
  - 5. Methodology
    - Presents a concise explanation of the theoretical study using a related diagram and discusses the design criteria and all required calculation steps in detail.
    - > Emphasis on the method of how you do the optimization.
    - > The reason for the method chosen.
  - 6. Data & Results, Discussion
    - Systematic result presentation. Use a table or graph when necessary.
    - Descriptive comment on each plot and discuss differences/similarities between theoretical and simulation results).
    - All labels on plots are clearly displayed and well-explained. Simulation results are accurate and precise. Observations are very thorough with comprehensive analysis and discussion
  - 7. Conclusion
    - Write a sample of conclusions for the problem/project (can also be in point form).
    - Generally, the conclusions should provide answers to the objectives stated earlier.
  - 8. References
    - Additional materials such as source codes, software or simulation programs etc. can be attached here.
    - > The cited references are reliable sources.