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SEEL3742

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STUDENT PACK

Device Simulation and Characterization of an n-channel MOSFET

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Project Introduction

Moore's law states that improving transistor performance, such as faster speed, smaller chip size, and lower power usage, is closely linked to scaling. Nevertheless, when the complementary metal oxide semiconductor (CMOS) transistor’s channel length is reduced to sub-100 nm, it causes short channel effects (SCEs), which include the threshold voltage roll-off and the drain-induced barrier lowering (DIBL). To address these limitations, various advanced process techniques are introduced, including lightly doped drain (LDD), halo implantation, and retrograde well doping in the transistor’s channel.

One issue that arises when scaling MOSFET devices is channel doping. If the channel is doped too lightly to achieve a low threshold voltage, punch-through can occur. As a result, channel doping needs to be increased, and oxide thickness must be reduced to address this issue while still maintaining sufficient inversion charge in the channel. However, reducing channel length and increasing substrate doping lead to another short channel effect known as impact ionization, where the drain/channel junction is reverse biased, and higher doping leads to a greater critical electric field in the device’s channel region.

1. Objectives

This laboratory is focused on the device characterization of an n-channel metal-oxide semiconductor field-effect transistor (n-MOSFET). NanoHUB software is used as the primary tool for the simulation work. NanoHUB will simulate the n-MOSFET device structure and device characteristic (I-V curve).

The objectives of this project are:

1. To simulate a device structure of an n-MOSFET using 90 nm technology and obtain its current-voltage curve (I_D-V_D and I_D-V_G).
2. To study the effect of channel length reduction on the device performance.
3. To characterize the electrical parameter of the n-MOSFET.
4. To optimize the device performance by changing the physical dimension/structure to reduce the short channel effects (SCEs).

2. Project Task

Suppose you are working in a semiconductor company that produces integrated circuit (IC) chips. As an engineer in the research and development (R&D) unit, you are assigned a specific task to investigate the performance of 90 nm CMOS as the next potential nanoscale device before being implemented into actual fabrication and mass production process. Many design aspects must be considered when the MOSFET device is scaled down into nanoscale regime. As channel length is scaled to smaller dimensions, gate oxide must be reduced in thickness. Due to these, the short channel effect and leakage problem become more significant and thus introduce a big challenge to increase the transistor's electrical performance.

You have decided to start with the simulation of an n-type MOSFET.

3. Instruction:

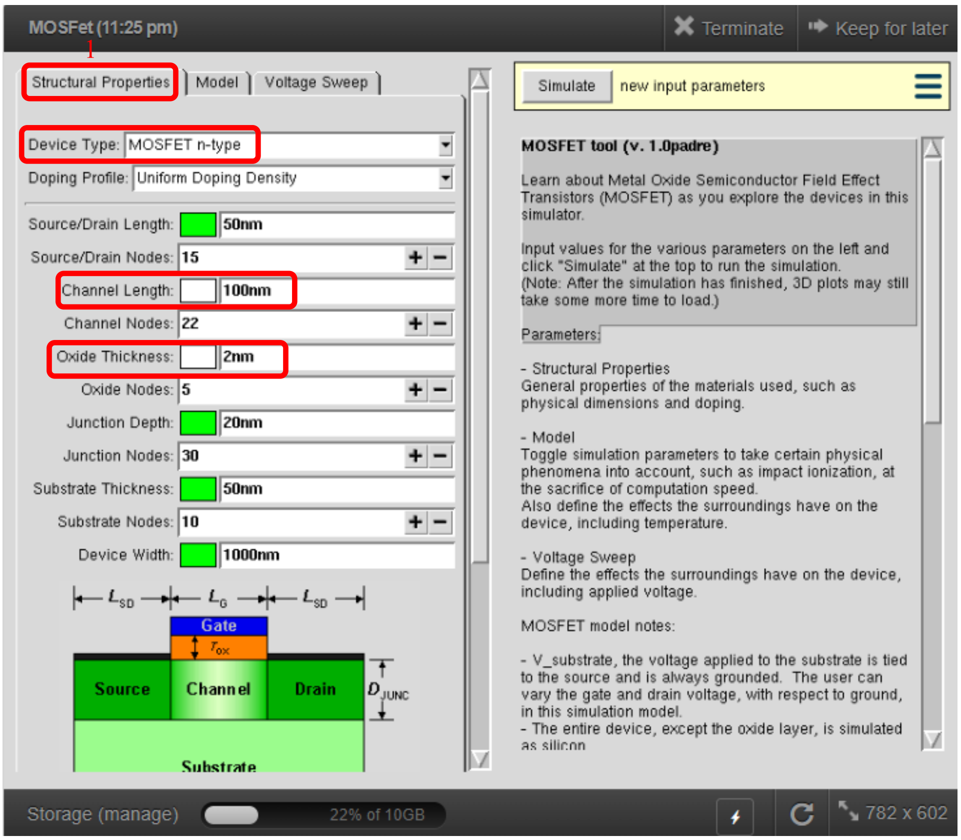
1. Simulate a MOSFET device structure by using MOSFET simulator on nanoHUB.org (http://nanohub.org/resources/mosfet). Before you can use the simulator, please sign up for the NanoHUB.
2. Follow the lab sheet on how to get started with NanoHUB (see **Appendix 1**).
3. Simulate the n-channel MOSFET device structure and fill up the device parameters according to the lab task given (see **Appendix 2**).
4. Take the reading of I-V curves (for both I_D-V_D and I_D-V_G) which you can download the .csv data.
5. Compile the schematic of the n-MOSFET device structure, the related I-V curves plots (for both I_D-V_D and I_D-V_G), the electrical properties (V_{th}, SS, I_{on} and I_{off}) for the n-channel MOSFET by using Origin or Matlab or any suitable software into word document together with all your results.
6. The electrical parameter for threshold voltage (V_{TH}), subthreshold slope (SS), drain-induced barrier lowering (DIBL), and on-current (I_{ON}) and off-current (I_{OFF}) are as follows:
   From the Log I_D-V_G plot, (V_{D1} = 0.05V for linear region and V_{D2} = 1.0V for saturation region).

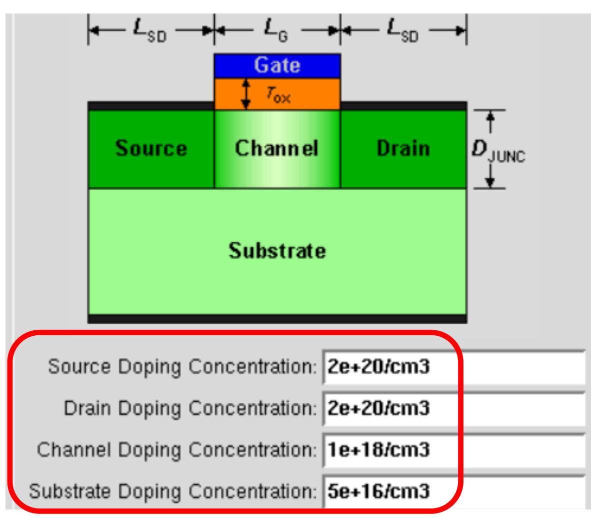
   - Threshold voltage, $V_{th} = V_G$ @ $I_D = 10^{-6}$A for V_{D2} = 1.0V.
   - Subthreshold slope, SS = ΔV_G @ the steepest 1 decade.
   - Leakage current, $I_{off} = I_D$ @ V_G = 0V for V_{D2} = 1.0V.
   - On saturation current, $I_{on} = I_D$ @ $V_G = V_{max}$ = 1V for V_{D2} = 1.0V.
   - Drain-induced barrier lowering, DIBL = (V_{th} @ V_{D1} = 0.05V – V_{th} @ V_{D2} = 1.0V) / (ΔV_D).

7. Please follow the timeline given in **Appendix 3** to complete your 3 weeks of the laboratory.

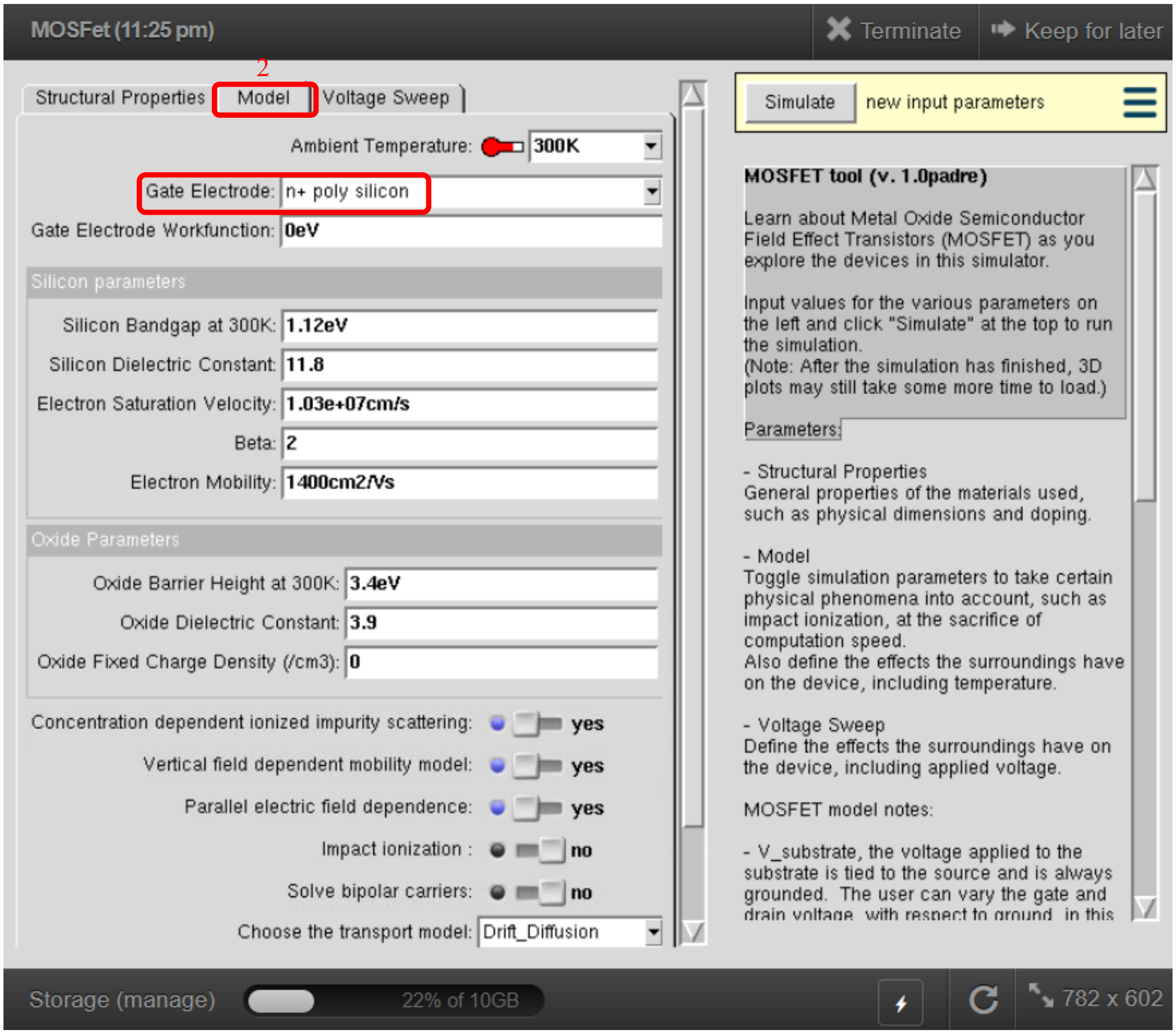
Appendix 1 (Lab sheet)

1. Sign up to NanoHub: http://nanohub.org/resources/mosfet
2. The GUI looks like this for the first tab menu: Structure Properties.
3. The red boxes are the device parameters that you should be focused on for your Lab Task. (Note: Other parameters which are not in the red boxes, keep it the same as the default value)
4. For this exercise, just leave it all as by Default value.

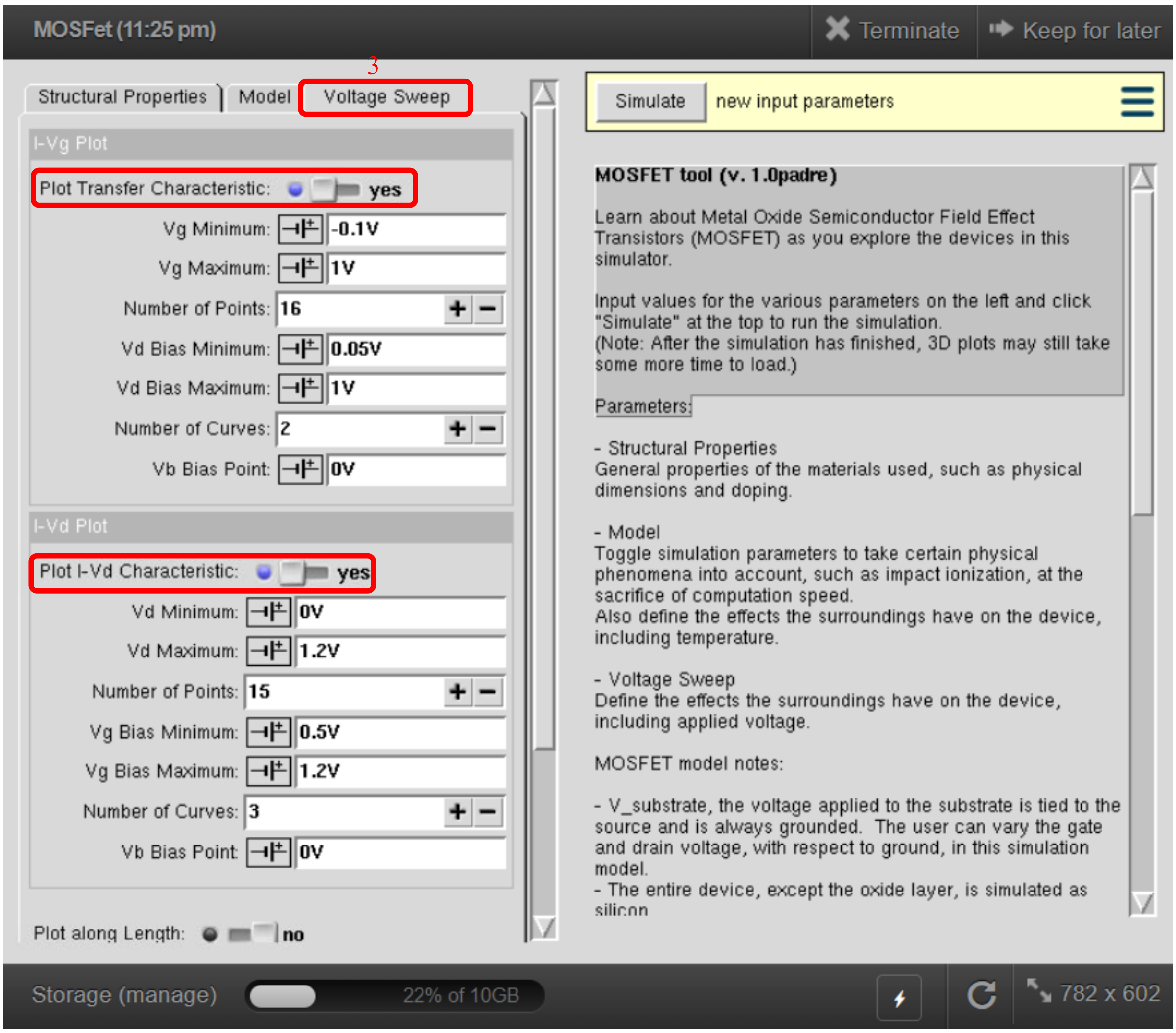




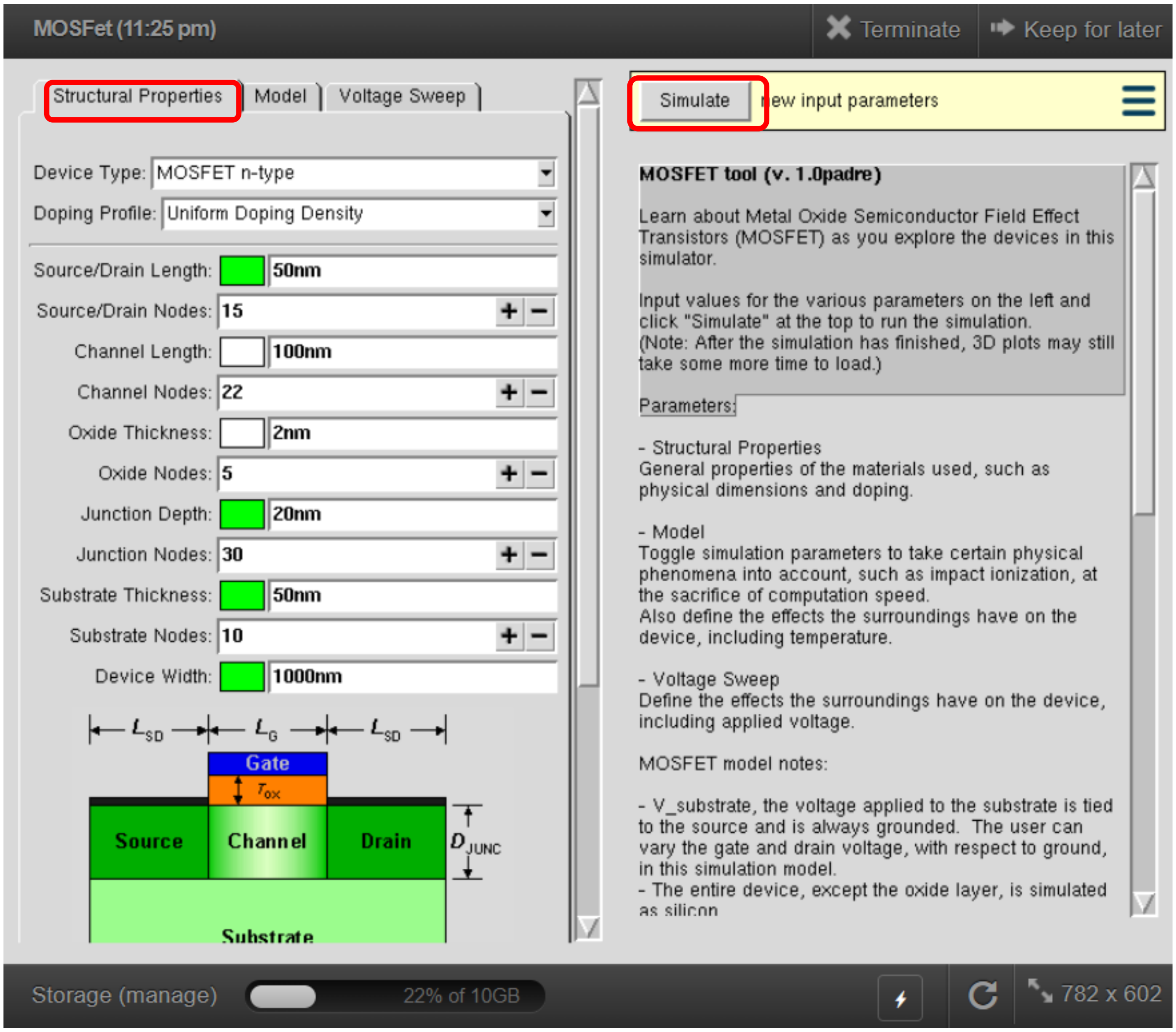
5. Click on the second tab menu. The GUI looks like this for the second tab menu: Model.
6. The red boxes are the device parameters that you should be focused on for your Lab Task. (Note: Other parameters which are not in the red boxes, keep it the same as the default value)
7. For this exercise, just leave it all as by Default value.



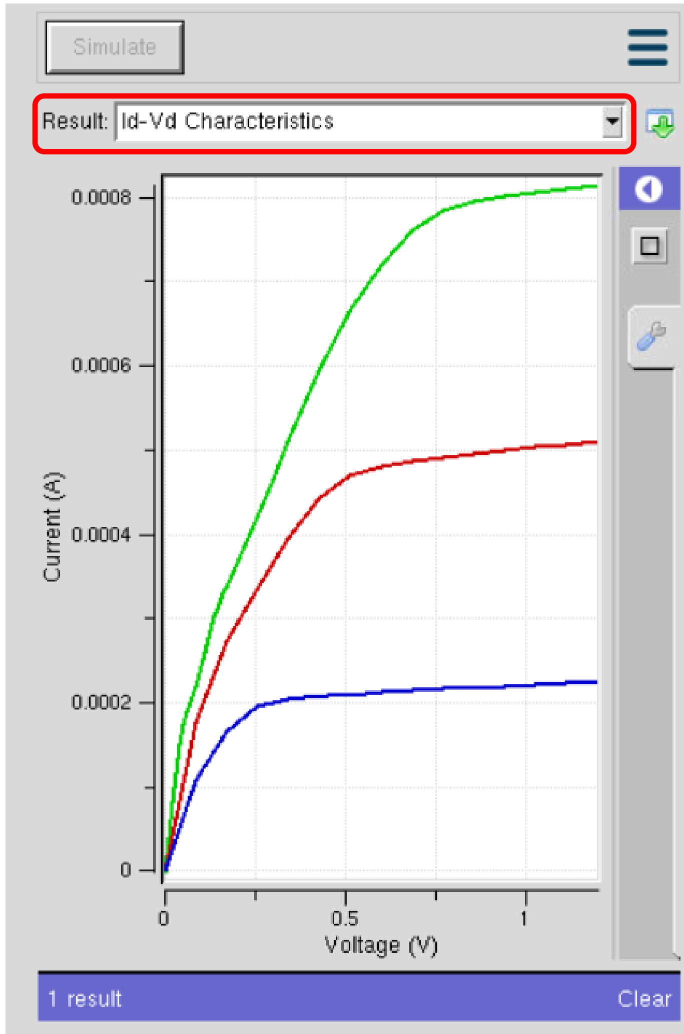
8. Click on the third tab menu. The GUI looks like this for the third tab menu: Voltage Sweep.
9. The red boxes are the device parameters that you should be focused on for your Lab Task.
10. For this, please tick "yes" for Plot I-Vd Characteristic. Other value, just leave it all as by Default value.



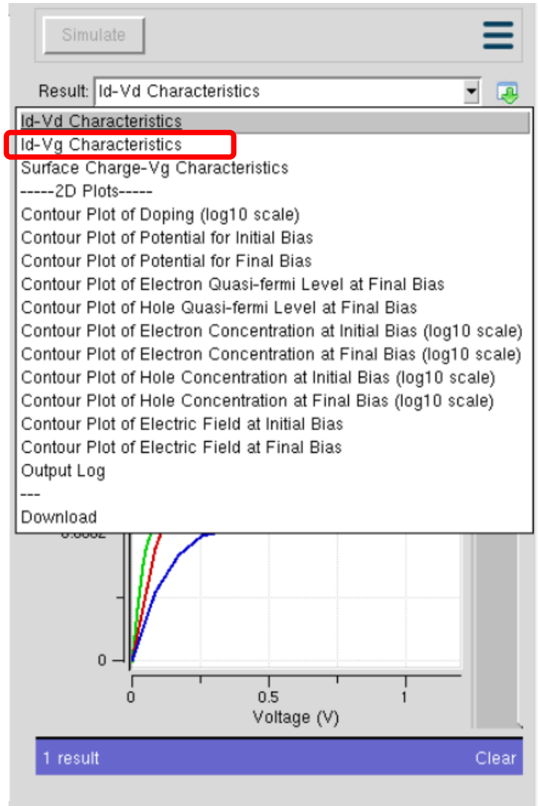
11. Go back to first tab menu: Structural Properties. Once all the parameter values have been set, to run the simulation, click "Simulate" button.

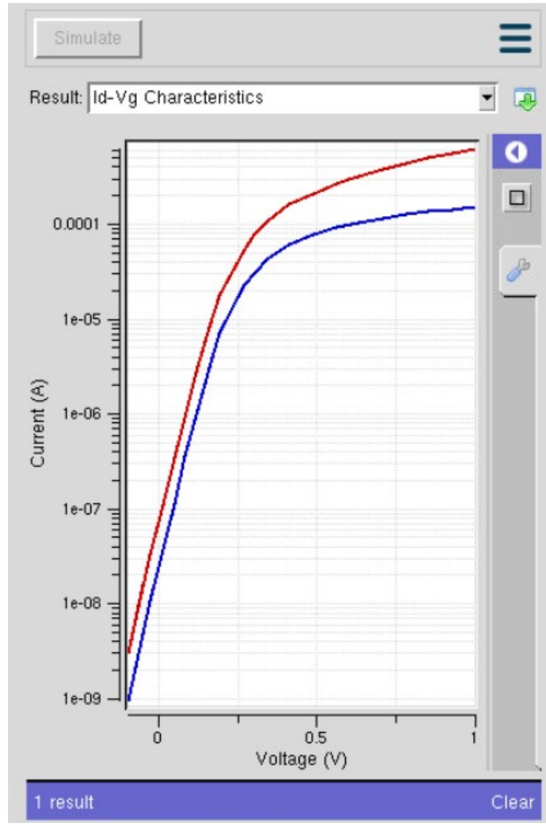


12. The results of the simulation will be appeared.
13. For I_D-V_D curve, choose Id-Vd Characteristics.

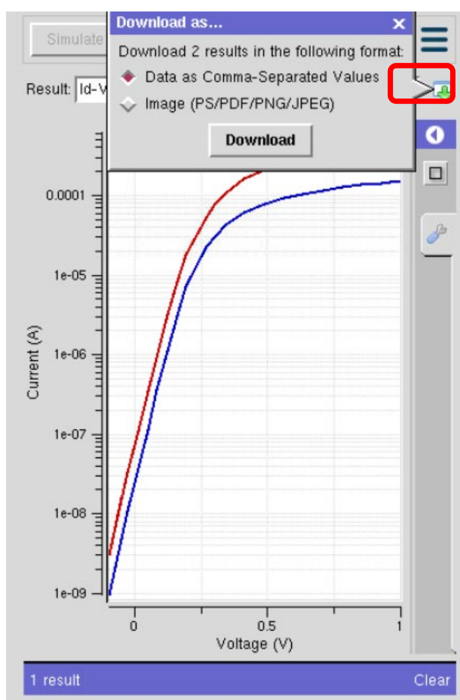


14. For I_D-V_G curve, scroll down menu and choose Id-Vg Characteristics. The graph is in Log scale I_D-V_G curve.





15. Click on the green arrow to get the data in .csv file. Click Download. You can replot your graph.



16. Analyze the electrical parameters. From the Log I_D-V_G plot, (V_{D1} = 0.05V for linear region and V_{D2} = 1.0V for saturation region).

- Threshold voltage, $V_{th} = V_G$ @ $I_D = 10^{-6}$A for V_{D2} = 1.0V.
- Subthreshold slope, SS = ΔV_G @ the steepest 1 decade.
- Leakage current, $I_{off} = I_D$ @ V_G = 0V for V_{D2} = 1.0V.
- On saturation current, $I_{on} = I_D$ @ $V_G = V_{max}$ = 1V for V_{D2} = 1.0V.
- Drain-induced barrier lowering, DIBL = (V_{th} @ V_{D1} = 0.05V – V_{th} @ V_{D2} = 1.0V) / (ΔV_D).

Appendix 2 (Lab Task)

1. In this lab task, you are required to simulate three generations (varying 3 channel lengths) of devices with parameters specified in Figure 1 and Table 1 without impact ionization included in the model, and set the voltage sweep as Default.

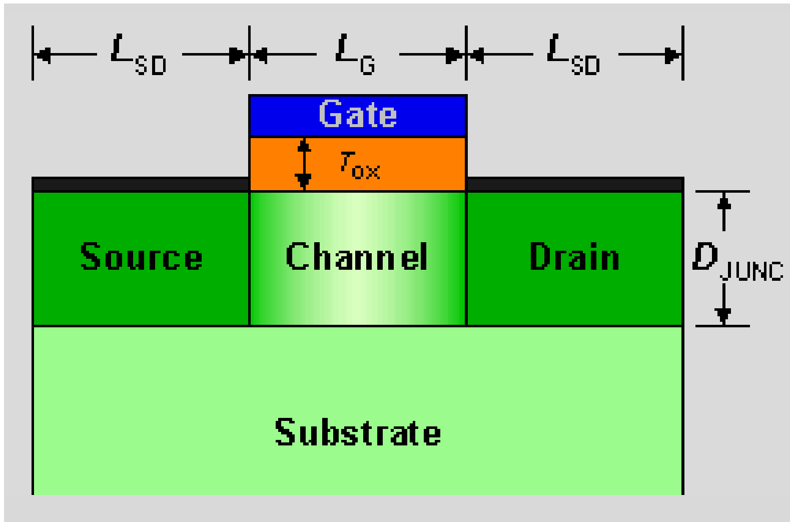


Figure 1: MOSFET Device structure.

Table 1: List of Device parameters with channel length variations

Device	Channel Length (nm)	Oxide thickness (nm)	Source/Drain Doping (cm^{-3})	Channel Doping (cm^{-3})	Substrate Doping (cm^{-3})	Gate electrode	V_G V_{DD} (V)
1	100	3	2×10^{20}	10^{18}	10^{17}	N+ Polysilicon	Default value
2	60	2	2×10^{20}	10^{18}	6×10^{17}	N+ Polysilicon	Default value
3	45	2	2×10^{20}	10^{18}	6×10^{17}	N+ Polysilicon	Default value

2. From the simulation results obtained, answer the following questions:

    a. Find the electrical properties for all the devices such as V_{th}, I_{on}, I_{off}, SS and DIBL for all the devices. Are all these devices well-designed, Yes or No? Please justify your answer with either Yes or No.
    b. From your observations and results of Device 3, what causes the I-V characteristics to behave differently from Devices 1 and 2. Discuss this phenomenon and please suggest how to overcome the issues.

3. For your next task, you need to do an optimization for Device 3, your 45 nm device should obtain the value of threshold voltage (V_{TH}) approximately of $V_{TH} \leq 0.3V$ and subthreshold slope, $SS \leq 85mV/dec$. Not only that, but you also need to optimize other parameters such as DIBL and I_{ON}/I_{OFF} ratio.
    a. There are several methods to optimize the device structure. Tips: you can try to alter this physical parameter of the device structure such as:
        - Oxide thickness
        - Substrate doping
        - Source/Drain Doping
        - Channel Doping
        - Gate Electrode
        - Or you can also use different Device types for example Double Gate MOSFET, SOI MOSFET, or any other device type that is available in the NanoHUB software.
    b. Simulate the I-V characteristics (for both I_D-V_D and I_D-V_G) of the optimized Device 3 and analyze the electrical parameters. Comment on the results obtained and justify the method that you choose for the optimization.

Appendix 3 (Timeline)

Week	Task	Interview	Submission Date
1	i. Understand the Lab instruction. ii. Follow the Lab sheet (Appendix 1). Simulate the I-V curves. Do characterization of the electrical parameter. Find V_{th}, I_{on}, I_{off}, SS, and DIBL. iii. Understand the Lab task (Appendix 2). Complete tasks No. 1 to 2. iv. Prepare Group proposal for task No. 3. v. Prepare Individual Short Report.	Respective Member	For Group Proposal and Individual short Report: Week 2
2	i. Submit Group Proposal and Individual Short Report. ii. Start to simulate task No. 3. iii. Simulate the I-V curves. Do optimization and characterization of the electrical parameter. Find V_{th}, I_{on}, I_{off}, SS, and DIBL.	Respective Member	-
3	i. Continue simulation work. ii. Group Demo. Present your results for optimized Device 3. Make a comparison between before and after optimization for Device 3. iii. Finalize Long Report.	Respective Member	For Long Report: A week after Week 3.

Guideline for Long Report

- ✓ Students must be able to present the report with all the required contents. Information is very organized, clear, and unambiguous with no mistakes. The report is orderly and visually appealing with no grammatical or spelling errors. All tasks were completed.
- ✓ The report follows the format (Outline: Abstract, Introduction/ Theory, Procedure, Data & Results, Discussion, Conclusion, and References).

1. Abstract
   - ➢ Must include the background, the problem statement, the objective, the methodology, and the significant findings.
2. Introduction/Theory
   - ➢ Background of problem/project.
   - ➢ The approach taken in solving the problem/project.
   - ➢ Introduction to MOSFET and advanced MOSFET devices and short-channel effects.
   - ➢ Design criteria of the MOSFET and advanced MOSFET device structures (depending on your choice of the optimized device).
3. Procedure
   - ➢ Emphasis on the lab procedure. Steps taken or methods used in conducting the simulation that can solve the problem/project.
   - ➢ May also include NMOSFET structure, parameters, characteristics etc.
   - ➢ Manual determination from graphs or equations
4. Objective
   - ➢ Objectives of the work (in the student's own words).
5. Methodology
   - ➢ Presents a concise explanation of the theoretical study using a related diagram and discusses the design criteria and all required calculation steps in detail.
   - ➢ Emphasis on the method of how you do the optimization.
   - ➢ The reason for the method chosen.
6. Data & Results, Discussion
   - ➢ Systematic result presentation. Use a table or graph when necessary.
   - ➢ Descriptive comment on each plot and discuss differences/similarities between theoretical and simulation results).
   - ➢ All labels on plots are clearly displayed and well-explained. Simulation results are accurate and precise. Observations are very thorough with comprehensive analysis and discussion
7. Conclusion
   - ➢ Write a sample of conclusions for the problem/project (can also be in point form).
   - ➢ Generally, the conclusions should provide answers to the objectives stated earlier.
8. References
   - ➢ Additional materials such as source codes, software or simulation programs etc. can be attached here.
   - ➢ The cited references are reliable sources.