

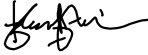

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**FAKULTI KEJURUTERAAN ELEKTRIK  
UNIVERSITI TEKNOLOGI MALAYSIA  
KAMPUS SKUDAI  
JOHOR**

**SKEL 3742  
VLSI SYSTEM DESIGN LAB**

**Lab Project 2: Traffic Light System**

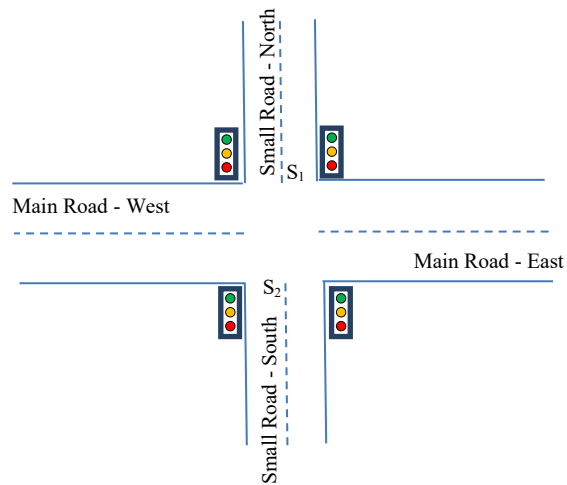
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## Project Introduction

A traffic light at a junction between the main road and a small road is controlled by two motion sensors ( $S_1$  and  $S_2$ ) as shown in Figure 1 below. The traffic light system has specifications as below: -

- 1) If both sensors are activated at the same time, the sensor with higher priority will take the first turn to green.
- 2) The period for green light for the main road ( $t_{G-main}$ ) is longer than the small road ( $t_{G-small}$ ).
- 3) For all junctions, the red light must turn on for a certain period ( $t_R$ ) before the green light for a particular junction can be turned on.
- 4) If the main road in green light and the sensors  $S_1$  and  $S_2$  detected no vehicle at the small road, the light at the main road will remain green.
- 5) The light for main road will turn from green to yellow when the period for green light is over.
- 6) The light will turn from yellow to red when the period for yellow light is over.
- 7) The light at the small road will turn from red to green if: -
  - a. The sensor detected there are vehicle at the small road **AND**
  - b. The period for all lights in red is over.
- 8) The light at the small road will turn from green to yellow if: -
  - a. The sensor detected no vehicle even though the period for green for the small road is still available **OR**
  - b. The period for the green light for the small road is over.
- 9) The light at any junction will turn yellow for a certain period ( $t_Y$ ) before turning red.
- 10) The period for yellow light is longer than that for red.

The traffic light system is to be designed and implemented but several things need to be determined such as the complete traffic sequence, the timing requirement ( $t_{G-main} > t_{G-small} > t_Y > t_R$ ) and the sensors' priority.



**Figure 1:** Traffic Light System

The objectives of this project are:

1. To design the traffic light system using a combinational and sequential logic design based on project specifications.
2. To draw the combinational and sequential logic circuit of the traffic light system using schematic design entry/hardware design language (HDL) coding and verify its function using Altera Quartus II Tools software.
3. To prototype and demonstrate the design of the system using Altera FPGA DE2 board.

## **Project Task**

Design the traffic light system using Quartus II schematic entry/HDL coding and FPGA development board. A report with the well-presented design steps, simulation results, and FPGA prototyping methodology is expected to be produced at the end of the project after the third session of the lab.

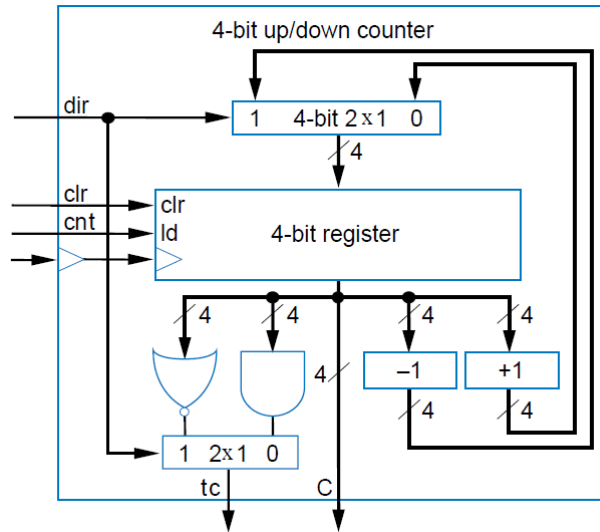
### **Some design guidelines:**

1. Design a circuit for the traffic light using multiplexers, counters, adders and similar logic blocks.
2. For your design, use appropriate gates, components and mega functions from the Quartus II system library.
3. Use counter to do count-down or count-up for the traffic light change.
4. Use registers or flip-flops for storage.
5. The motion sensor inputs will eventually be connected to the toggle switches on the DE2 board.
6. The countdown for the traffic light will eventually be displayed on the 7-segment displays on the DE2 board.

Identify the input and output of your system, encoding method, circuit topology and suitable algorithm to be used. Design the system using combinational and sequential logic and verify the design using Quartus II CAD Tool. Final task is to prototype and demonstrate your system using FPGA DE2 board. Refer to Quartus II and FPGA tutorial to help you to implement this project.

### Week 1:

Design the traffic light system including a block diagram for the datapath and a state machine diagram for the control unit. Figure 2 shows a sample of the datapath unit for your reference. Use this as an example (modify) to design your datapath.



**Figure 2:** Up/Down Counter (F. Vahid, Chapter 4, Digital Design, 2006)

### Week 2:

Design the datapath and control unit using schematic entry or Verilog HDL. Verify your design by using a simulation waveform to check design correctness.

### Week 3:

Implement the completed traffic light on the Altera DE2 FPGA board. Use the toggle switches for input and 7-segment display as well as LEDs for output.